M62021L,P,FP

SYSTEM RESET IC WITH SWITCH FOR MEMORY BACK-UP

DESCRIPTION

The M62021 is a system IC that controls the memory backup function of SRAM and microcomputer (internal RAM).
The IC outputs reset signals(RES/$\overline{RES}$) to a microcomputer at power-down and power failure.It also shifts the power supply to RAM from main to backup,outputs a signal ($\overline{CS}$) that invokes standby mode,and alters RAM to backup circuit mode.
The M62021 contains,in a single chip,power supply monitor and RAM backup functions needed for a microcomputer system,so that the IC makes it possible to construct a system easily and with fewer components compared with a conventional case that uses individual ICs and discrete components.

FEATURES

- Built-in switch for selection between main power supply and backup power supply to RAM.
- Small difference between input and output voltage (I_{OUT}=80mA,V_{IN}=5V)0.2V typ
- Detection voltage (power supply monitor voltage)4.40V±0.2V
- Chip select signal output($\overline{CS}$)

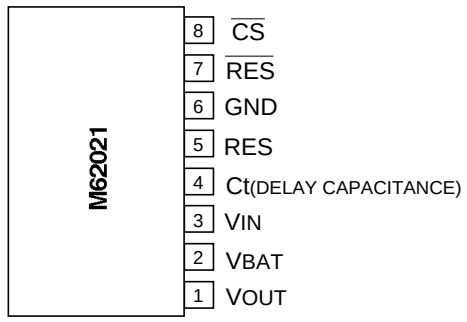
Two channels of reset outputs(RES/$\overline{RES}$)

- Power on reset circuit built-in
- Delay time variable by an external capacitance connected to Ct pin
- Facilitates to form backup function with a few number of components

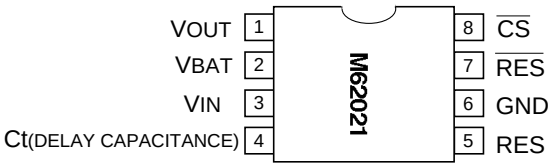
APPLICATION

Power supply control systems for memory backup of microcomputer system and SRAM boards with built-in backup function that require switching between external power supply and battery.

PIN CONFIGURATION (TOP VIEW)

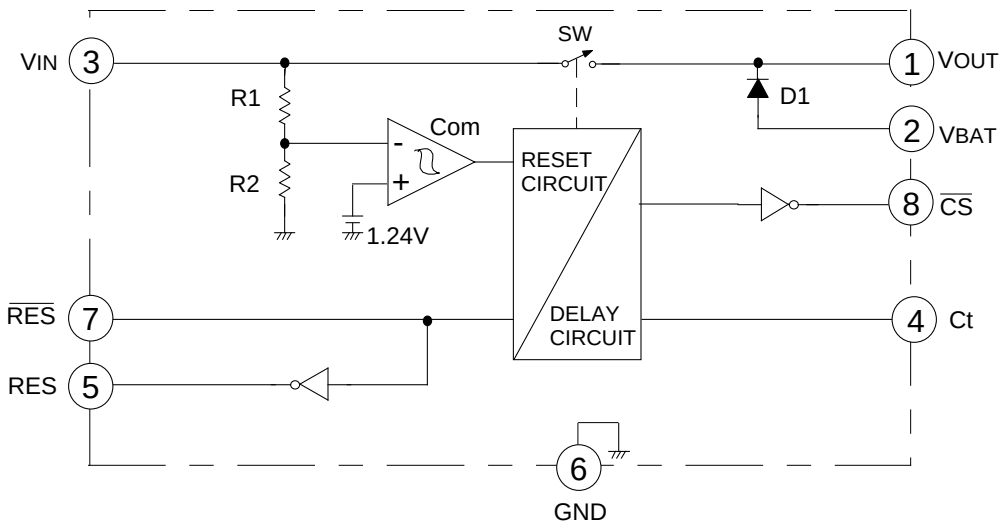


Outline 8P5(L)



Outline 8P4(P)
8P2S-A(FP)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

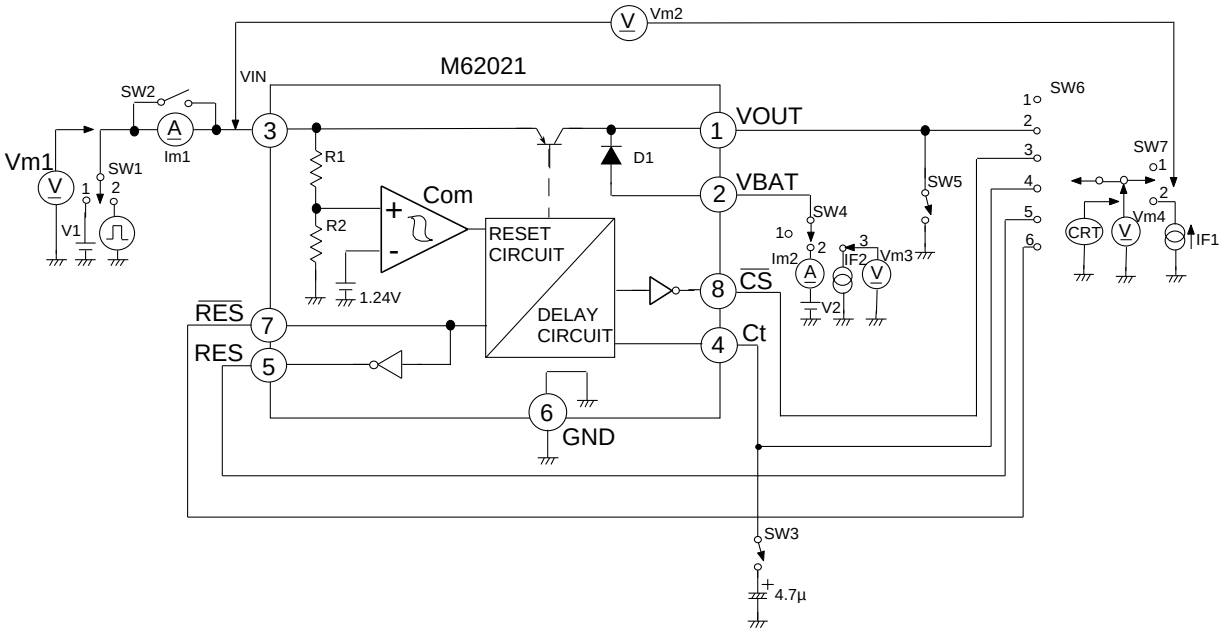
Symbol	Parameter	Conditions	Ratings	Unit
V_{IN}	Input voltage		7	V
I_{OUT}	Output current		100	mA
Pd	Power dissipation		800(SIP)/625(DIP)/440(FP)	mW
K_Θ	Thermal derating	(Ta≥25°C)	8(SIP)/6.25(DIP)/4.4(FP)	mW/°C
T_{opr}	Operating temperature		-20 ~ +75	°C
T_{stg}	Storage temperature		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
Vs	Detection voltage	V_{IN}(At the change from H →L)		4.2	4.4	4.6	V
ΔVs	Hysteresis voltage	ΔVs=V_{SH}-V_{SL}		50	100	200	mV
Vs/ΔT	Temperature coefficient of detection voltage				0.005		%/°C
I_{CC}	Circuit current	I_{OUT}=0mA	V_{IN}=4V		2.0	4.0	mA
			V_{IN}=5V		7.5	12.0	
V_{DROP}	Difference between input and output voltage	V_{IN}=5V	I_{OUT}=50mA		0.125	0.25	V
			I_{OUT}=80mA		0.2	0.4	
V_{OH}(Ct)	Ct output voltage (high level)	V_{IN}=5V(Note1)		4.5	5.0		V
V_{OL}(Ct)	Ct output voltage (low level)	V_{IN}=4V(Note1)			0.02	0.1	V
V_{OH}(RES)	RES output voltage (high level)	V_{IN}=4V(Note1)		3.5	4.0		V
V_{OL}(RES)	RES output voltage (low level)	V_{IN}=5V	(Note1)		0.02		V
			I_{SINK}=1mA		0.05	0.2	
V_{OH}($\overline{RES}$)	$\overline{RES}$ output voltage (high level)	V_{IN}=5V(Note1)		4.5	5.0		V
V_{OL}($\overline{RES}$)	$\overline{RES}$ output voltage (low level)	V_{IN}=4V	(Note1)		0.02		V
			I_{SINK}=1mA		0.05	0.2	
V_{OH}($\overline{CS}$)	$\overline{CS}$ output voltage (high level)	V_{IN}=4V (Note2)		3.50	3.57		V
		V_{IN}=0V,V_{BAT}=3V (Note2)		2.40	2.47		
V_{OL}($\overline{CS}$)	$\overline{CS}$ output voltage (low level)	V_{IN}=5V	(Note1)		0.08		V
			I_{SINK}=1mA		0.1	0.3	
I_R	Backup Di leak current	V_{BAT}=3V	V_{IN}=5V			±0.5	μA
			V_{IN}=0V			±0.5	
V_F	Backup Di forward direction voltage	I_F=10μA			0.54	0.6	V
tpd	Delay time	V_{IN}=0V →5V,Ct=4.7μF		10	27	55	ms
td	Response time	V_{IN}=5V →4V			5.0	25.0	μs
V_{OPL}($\overline{RES}$)	$\overline{RES}$ limit voltage of operation	(Note 3)			0.65		V

Note 1.Regarding conditions to measure V_{OH} and V_{OL},voltage values are to be generated by internal resistance only and no external resistor is used.
2.These values are produced inserting an external resistor,$R\overline{CS}$=1MΩ,between the CS pin and GND.
3.With no external resistor (10kΩ internal resistance only)

TEST CIRCUIT



SWITCH MATRIX

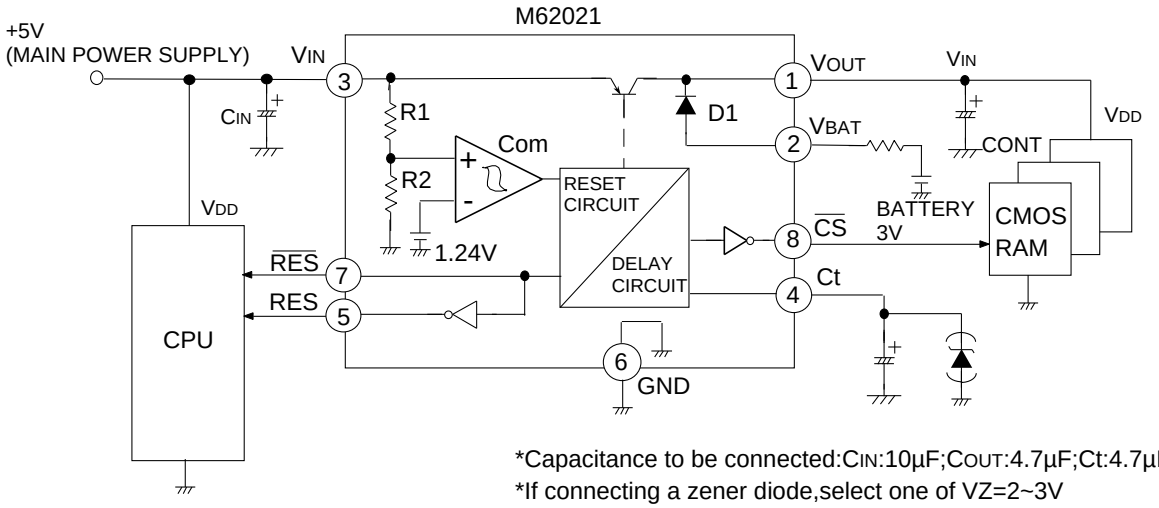
Symbol	Parameter		V1	V2	IF1	IF2	S W 1	2	3	4	5	6	7	Measuring instrument
Icc	Circuit current		4V 5V	–	–	–	1	ON	OFF	1	OFF	1	1	Im1
Vs (VSL)	Detection voltage (VIN negative-going)	VOUT CS Ct RES RES	Decrease from 5V	–	–	–	1	ON	OFF	1	OFF	2 3 4 5 6	1	(Note5) Vm4 CRT Vm1
VDROP	Difference between input and output voltage		5V	–	-50mA -80mA	–	1	ON	OFF	1	OFF	2	2	Vm2
VOH(Ct)	Ct output voltage(high level)		5V	–	–	–	1	ON	OFF	1	OFF	4	1	Vm4
VOL(Ct)	Ct output voltage(low level)		4V											
VOH(RES)	RES output voltage(high level)		4V	–	–	–	1	ON	OFF	1	OFF	5	1	Vm4
VOL(RES)	RES output voltage(low level)		5V		1mA								2	
VOH(RES)	RES output voltage(high level)		5V	–	–	–	1	ON	OFF	1	OFF	6	1	Vm4
VOL(RES)	RES output voltage(low level)		4V		1mA								2	
VOH(CS)	CS output voltage(high level)(Note 4)		4V 0V	3V	–	–	1	ON	OFF	1	OFF	3	1	Vm4
VOL(CS)	CS output voltage(low level)		5V	–	1mA								2	
IR	Backup Di leak current		5V 0V	3V	–	–	1	ON	OFF	2	OFF	1	1	Im2
VF	Backup Di forward direction voltage		0V	–	–	10µA	1	ON	OFF	3	ON	1	1	Vm3
tpd td	Delay time Response time	VOUT CS RES RES	–	–	–	–	2 (Note6)	ON	ON (Note7)	1	OFF	2 3 5 6	1	CRT

Notes 4.To measure VOH(CS),insert a 1MΩ resistor between the CS pin and GND.
5. While monitoring each output by Vm4 or CRT,measure the input voltage Vm1 when the output goes from H to L and L to H.Regarding VSH,raise VIN from 4V and measure the input voltage Vm1 when the output goes from H to L and L to H.ΔVs is VSH-VSL.
6. To measure delay time, change VIN from 0V to 5V and compare,with respect to each pin,the positive-going edge observed on a monitor with that of VIN.To measure response time,change VIN from 5V to 4V and compare,with respect to each pin,the negative-going edge observed on a monitor with that of VIN.
7.Set the switch to OFF when measuring response time.

EXPLANATION OF TERMINALS

Pin No.	Symbol	Name	Function
①	V_{OUT}	Power supply output	V_{IN} and V_{BAT} are controlled by means of an internal switch and output through V_{OUT} The pin is capable of outputting up to 100mA.Use it as V_{DD} of CMOS RAM and the like
②	V_{BAT}	Backup power supply input	Backup power supply is connected to this pin If a lithium battery is used,insert a resistor in series for safety purposes
③	V_{IN}	Power supply input	+5V input pin.Connect to a logic power supply.
④	Ct	Delay capacitor connection pin	A delay capacitor is connected to this pin.By connecting a capacitor,it is possible to delay each output
⑤	RES	Positive reset output	Connect to the positive reset input of a microcomputer.The pin is capable of flowing 1mA sink current
⑥	GND	Ground	Reference for all signals
⑦	$\overline{RES}$	Negative reset output	Connect to the negative reset input of a microcomputer.The pin is capable of flowing 1mA sink current
⑧	$\overline{CS}$	Chip select output	Connect to the $\overline{\text{chip select}}$ of RAM.The CS output is at low level in normal state thereby letting RAM be active.Under failure or backup condition,the CS output is set to high level,then RAM enters standby state disabling read/write function.The pin is capable of flowing a 1mA sink current

APPLICATION EXAMPLE



*Capacitance to be connected:C_{IN}:10µF;C_{OUT}:4.7µF;Ct:4.7µF
*If connecting a zener diode,select one of VZ=2~3V

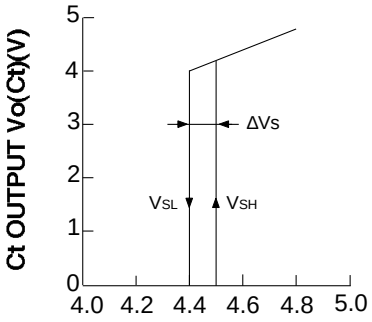
CONFIGURATION

<Power supply detector>

The internal reference voltage Vref is compared by means of a comparator with resistor-divided voltage VR(resistor-divided voltage produced by R1 and R2 from VIN).

If the input voltage is 5V,VR is set to 1.24V or higher,so the comparator output is at low level and the Ct output(Q1 collector output)is set to high level.If the input voltage drops to below 4.4V in an abnormal condition,VR becomes below 1.24V,so the comparator output goes from low to high level and the Ct output,from high to low.The input voltage at this point is called VSL.Next,when the input voltage,restored from abnormal state,has a rise,the comparator output goes from high to low level and the Ct output,from low to high.

The comparator used for detection has 100mV hysteresis(ΔVs),so that malfunctioning is prevented in case that the input voltage slowly drops or VR nearly equals Vref.



<Delay Circuit>

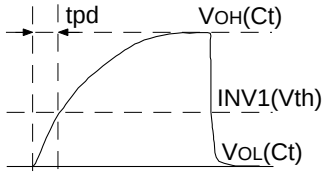
Connecting an external capacitor to the Ct pin lets RES,$\overline{RES}$,$\overline{CS}$,and VOUT be delayed due to RC transient phenomenon(electric charge).

Delay time is determined as follows.

$$\text{Delay time(tpd)} = Ct \times (R3 + R4) \times \ln \frac{[VOH(Ct)-VOL(Ct)]}{[VOH(Ct)-INV1(VTH)]}$$

$$= Ct \times 22k\Omega \times 0.2614$$

$$\fallingdotseq 5.75 \times 10^3 \times Ct \qquad \text{*Ct is an external capacitance.}$$



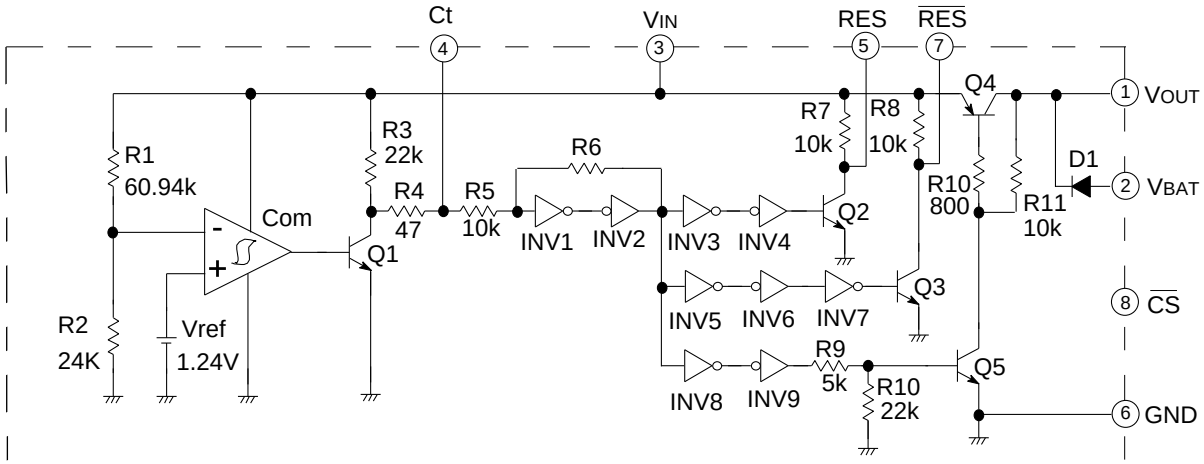
DELAYED OUTPUT WAVEFORMS OF Ct

Taking into consideration the time taken by the oscillator of microcomputer to be stable,connect a 4.7μF capacitor to the Ct pin.
(As the response time of detection can be slowed due to internal structure depending on the rising rate of power supply,avoid connecting a too large capacitance.

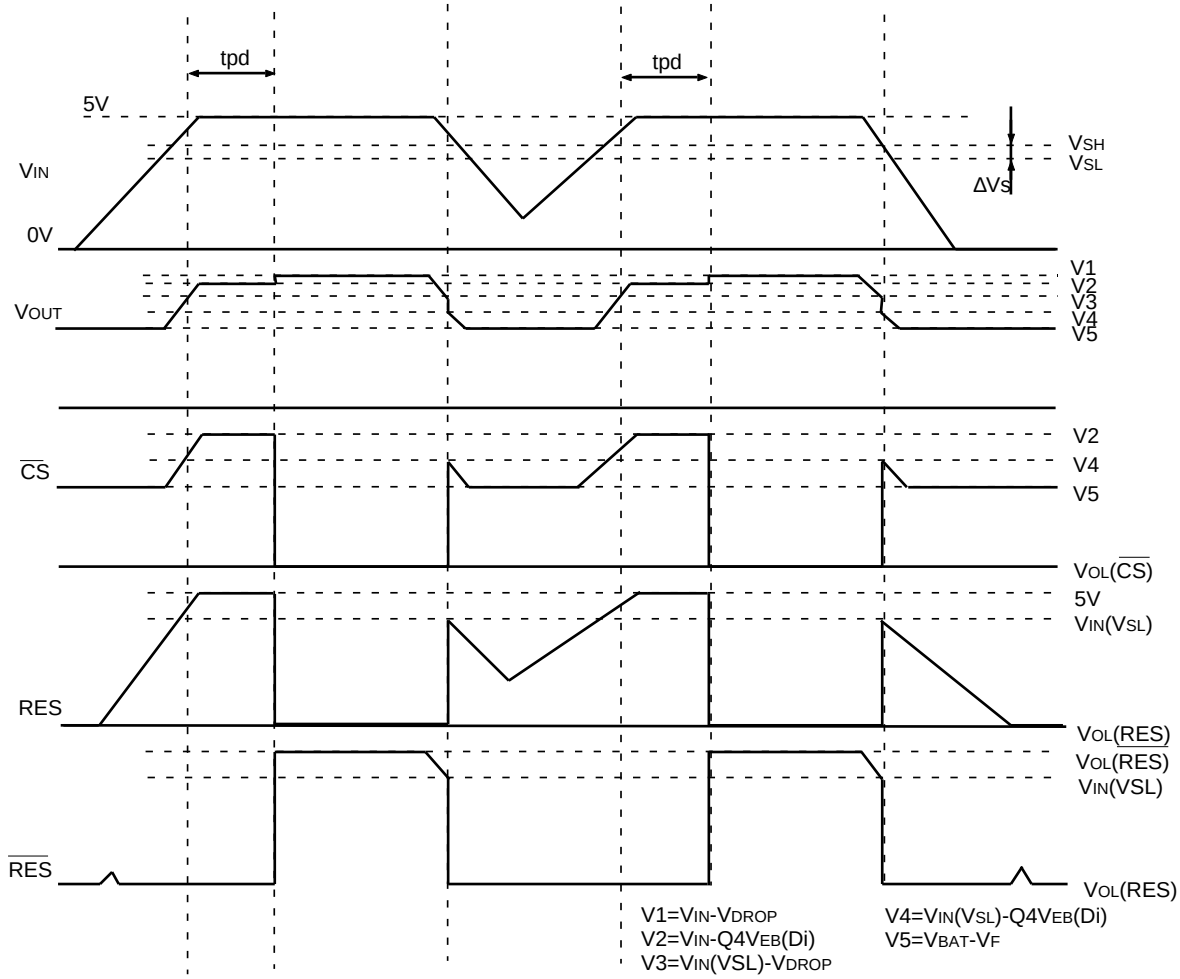
<Schmitt trigger circuit>

Since waveforms show a gentle rise due to the RC delay circuit,INV1,INV2,R5,and R6 constitute a schmitt trigger circuit to produce hysteresis so as to prevent each output from chattering.

INTERNAL CIRCUIT



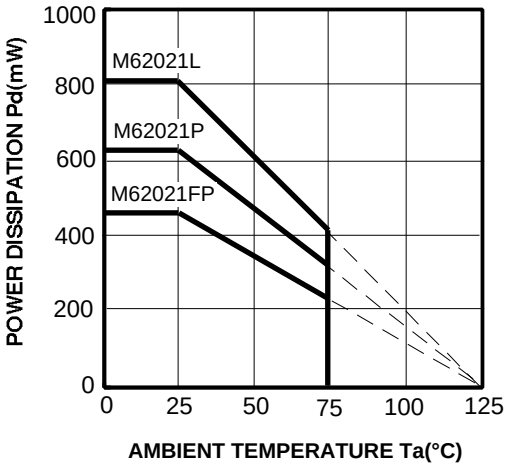
TIMING CHART



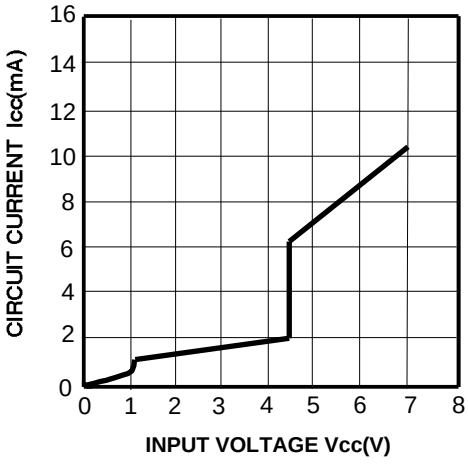
Input voltage / Output pin	In normal operation	In failure(instantaneous drop)	Restoration from failure (instantaneous drop)	In backup state
	Input voltage:5V	Input voltage:5V→4V Each output varies if the input voltage drops to VSL or under	Input voltage:4V→5V If the input voltage goes higher than VSL by 100mV,each out-put varies after delay produced by the delay circuit	Input voltage:0V Backup voltage:3V
VOUT	With Q4 set to ON, a voltage (VIN-VDROP)is output	Q4 is turned OFF.A voltage (VIN-Q4 VEB(Di) is output by the diode between E and B of Q4	Q4 is turned ON after delay and a voltage(VIN-VDROP) is output	VBAT-VF
RES	The output level is VOL(RES) with a logic low	As the state shifts from a logic low to logic high,the output level becomes approximately equal to the input voltage	A logic high is maintained,and than shifts to a logic high	———
$\overline{RES}$	The output level is VOH(RES) with a logic low	As the state shifts from a logic high to logic low,the output level becomes VOL(RES)	A logic low is held,and than shifts to a logic high	———
$\overline{CS}$	The output level is VOL(CS) with a logic low	As the state shifts from a logic low to logic high,the output level becomes the voltage VIN-Q4EB(Di).	A logic high is maintained,and than shifts to a logic high	The output is a logic high and the output level is VBAT-VF

TYPICAL CHARACTERISTICS

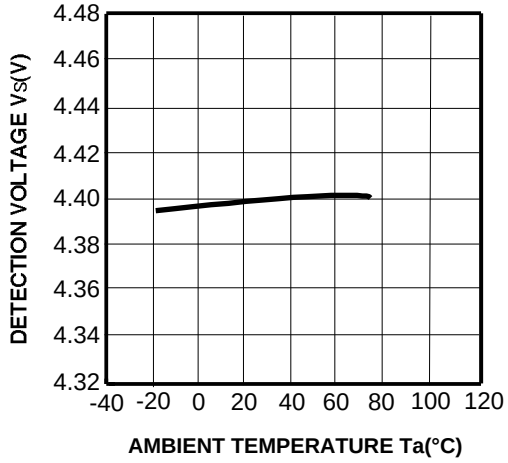
THERMAL DERATING (MAXIMUM RATING)



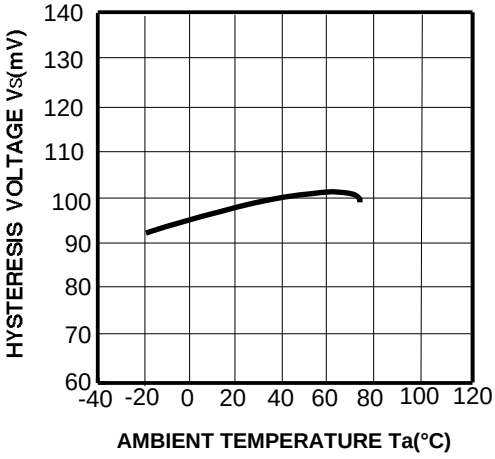
CIRCUIT CURRENT VS. INPUT VOLTAGE



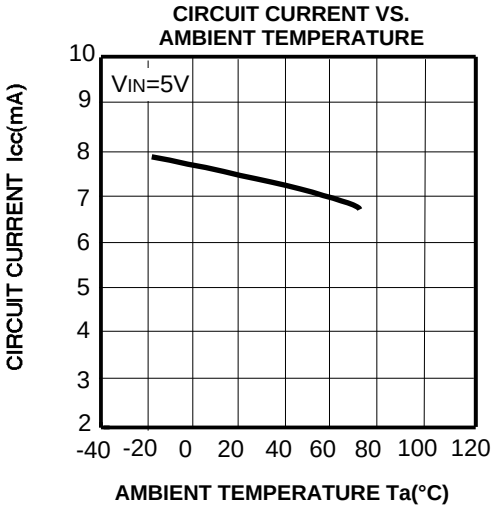
DETECTION VOLTAGE VS. AMBIENT TEMPERATURE



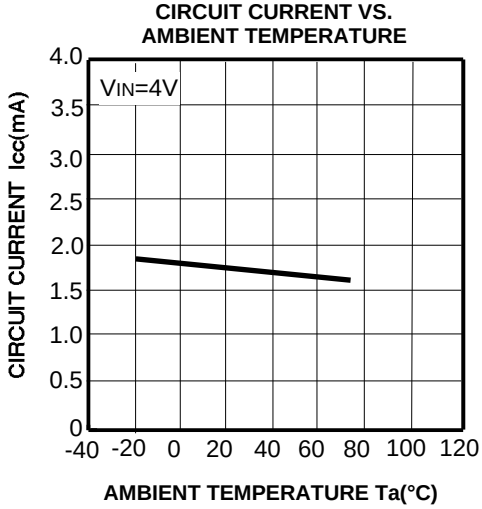
INTERRUPTION OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



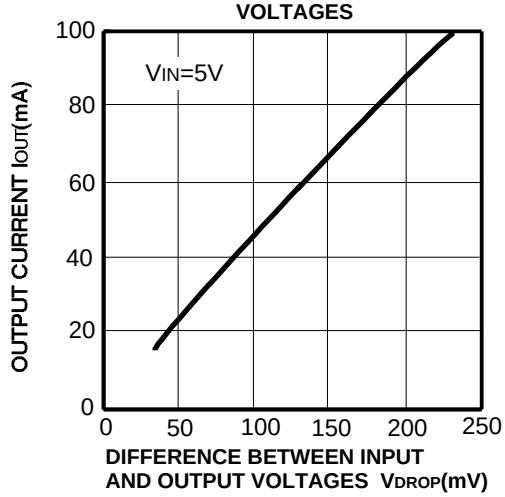
CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



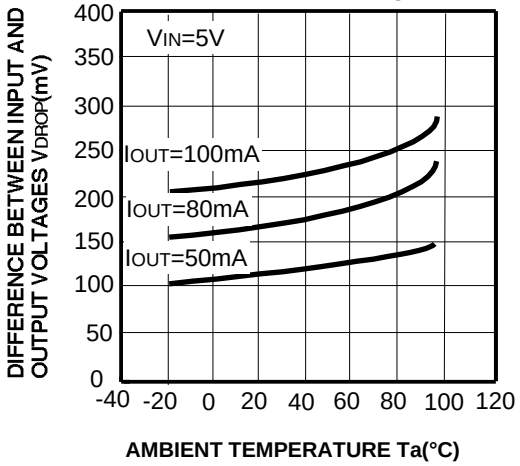
CIRCUIT CURRENT VS. AMBIENT TEMPERATURE



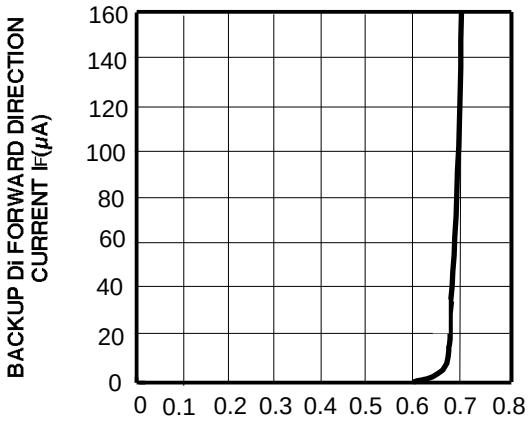
OUTPUT CURRENT VS. DIFFERENCE BETWEEN INPUT AND OUTPUT VOLTAGES



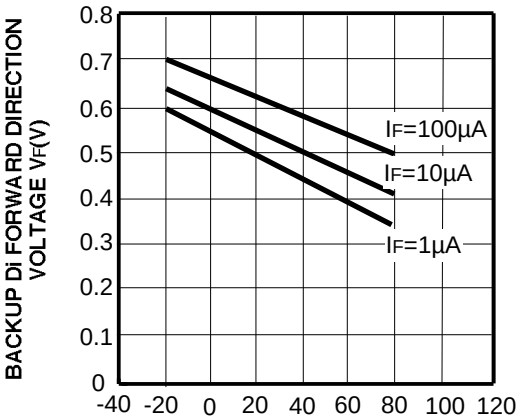
DIFFERENCE BETWEEN INPUT AND OUTPUT VOLTAGES VS. AMBIENT TEMPERATURE



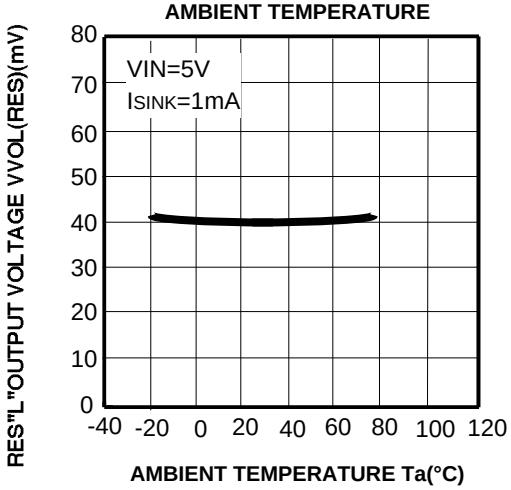
BACKUP Di FORWARD DIRECTION CURRENT VS. VOLTAGE



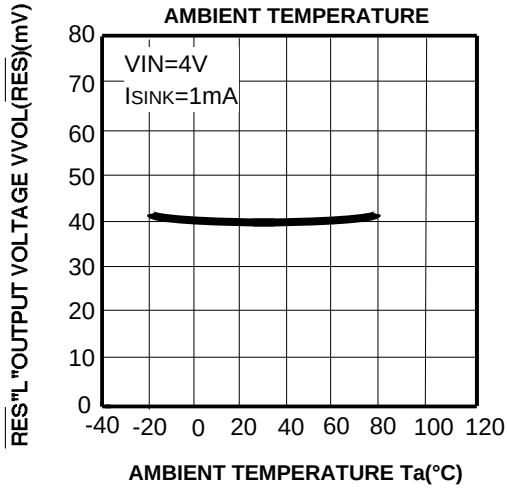
BACKUP Di FORWARD DIRECTION VOLTAGE VS. AMBIENT TEMPERATURE



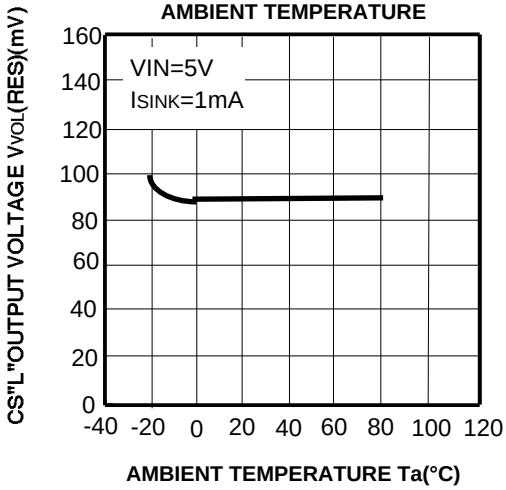
RES"L"OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



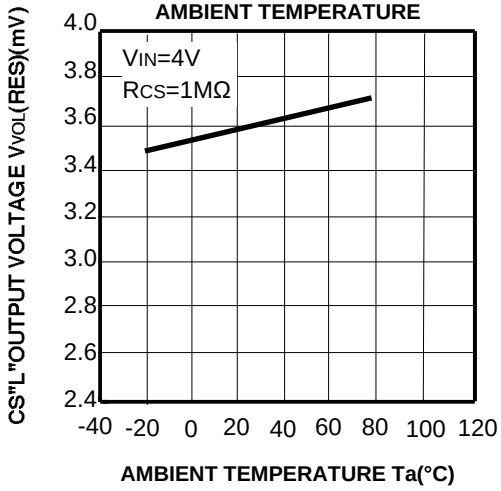
$\overline{RES}$ "L"OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



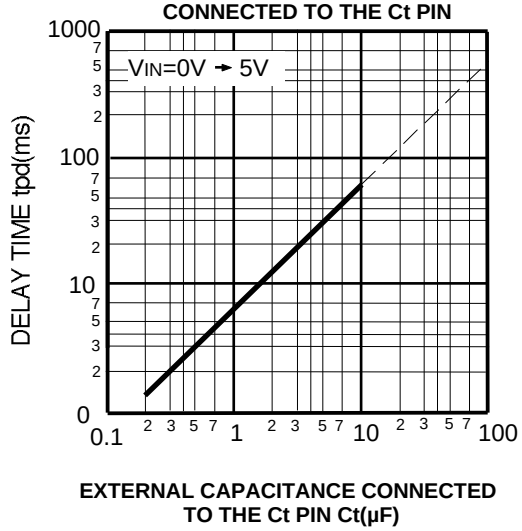
CS"L"OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



CS"L"OUTPUT VOLTAGE VS. AMBIENT TEMPERATURE



DELAY TIME VS.EXTERNAL CAPACITANCE CONNECTED TO THE Ct PIN



DELAY TIME VS.AMBIENT TEMPERATURE